Current-Aware Adaptive Dead-Time Control for Extended Zero Voltage Switching in Dual Active Bridge for EV Chargers

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Abstract

The adoption of electric vehicles (EVs) to address Sustainable Development Goals 7, 11, and 13 has driven the demand for high-efficiency, bidirectional charging units. The Dual Active Bridge (DAB) is the leading topology for charging units due to key features such as galvanic isolation, inherent Zero Voltage Switching (ZVS), and bidirectional power flow (V2G). However, traditional fixed dead-time control techniques bring critical trade-offs: satisfactory dead-time protects heavy loads but invariably results in excessive body diode conduction, while fixed dead-time fails to facilitate Zero Voltage Switching at light loads, leading to hard-switching losses. This research outlines a comprehensive, current-aware adaptive dead-time control technique that dynamically modulates the dead-time interval based on the real-time sensing of the transformer leakage current. By dynamically tuning the dead time (blanking interval), the proposed method extends the soft-switching operating range, minimises reverse conduction losses, and mitigates voltage waveform distortion. Validation through MATLAB/Simulink modelling including a 10 kW Electric Vehicle (EV) charger model demonstrates up to a 4.2% efficiency improvement under light to medium loads compared to conventional fixed dead-time techniques.

Keywords: Dual Active Bridge (DAB) Converter, Adaptive Dead-Time Control, Zero Voltage Switching (ZVS), Current-Aware Control Strategy, Switching Loss Reduction, Body Diode Conduction

1. INTRODUCTION

The wide adoption of electric vehicles (EVs) requires a robust, high-efficiency power electronics charging ecosystem. Modern developments in EVs, photovoltaic inverters, and battery storage systems have catalysed renewed interest in DAB converters [1, 2]. The Dual Active Bridge (DAB) converter comprises two full active bridges linked through a high-frequency transformer (HFT), providing safe and efficient bidirectional power transfer management [3]. Its widespread adoption is attributed to numerous benefits, including high power density wide voltage-range compatibility and soft-switching capabilities. Besides these benefits, DAB converters normally face operational restrictions because of reliance on static dead-time (t_{dt}) control techniques [4]. Dead time is a deliberate gap inserted between switching complementary MOSFETs to avoid catastrophic shoot-through [5]. Static t_{dt} parameters are the main driver of Zero Voltage Switching loss, pre-eminent switching losses, electromagnetic interference (EMI), and general efficiency degradation[6]. Operational conditions such as load current, switching frequency, and voltage ratio dictate the optimal dead-time duration, yet conventional designs often deploy fixed values tailored to a single, nominal operating point[7].

While adaptive dead-time techniques have been explored using off-line mathematical models, pure model-based schemes suffer from parametric drift, temperature dependence of MOSFET parasitic capacitances (C_{oss}), and transformer leakage inductance (L_{lk}) tolerances. Conversely, direct high-frequency current sensing introduces practical challenges, including low signal-to-noise ratios (SNR) during sub-microsecond switching transitions, sensor propagation delay, and phase-shift

distortion caused by variable dead-time step voids.

To overcome these limitations, this work presents a hybrid current-aware adaptive dead-time control scheme that combines real-time ADC current sampling with non-linear SiC switch $Q_{oss}(V_{ds})$ Look-Up Tables (LUTs) and an integrated phase-shift compensation loop ($\Delta\phi$), achieving robust ZVS extension down to light load conditions without incurring phase-leg shoot-through or control-loop power sag.

This paper addresses the existing research gap by proposing an adaptive, current-aware dead-time control strategy. The objective is to achieve a holistic system design that seamlessly integrates loss minimisation, ZVS robustness, and real-time digital implementability for EV charging applications.

2. DAB FUNDAMENTALS AND THE DEAD-TIME DILEMMA

A single-phase DAB converter consists of a primary switching full-bridge, a high-frequency transformer (HF-Tx), a leakage inductance (L_{lk}), and a secondary switching full-bridge as shown in Figure 1. The power transfer is controlled by the phase shift between the primary (Bridge 1) and secondary bridge (Bridge 2) voltages [8]. The DAB converter leverages high-frequency magnetic coupling to manage bidirectional power flow between two DC sources. The PWM Bridge 1 converts the incoming DC voltage into a high-frequency square wave or quasi-square wave voltage $(v_P(t))$. This AC $v_{pt}(t)$ signal then passes through the L_{lk}, which serves as the primary energy storage and transfer medium for the entire system. The principle of operation is based on the Phase Shift (ϕ) between the switching patterns of the two bridges. Simultaneously, the PWM Bridge 2 generates $v_s(t)$, which is reflected to the primary side as $nv_s(t)$. Unlike traditional converters that modulate the duty cycle, a DAB typically operates with a fixed 50% duty cycle for all switches [9] [26]. Instead, the controller introduces a time delay in the phase shift between the primary bridge and the secondary bridge. When Bridge 1 leads Bridge 2, the phase shift creates a voltage across the leakage inductor that transfers power from input to output. Reversing the phase so that Bridge 2 leads invert the current direction, enabling power flow back to the source [10]. The high-frequency transformer (HFT) provides galvanic isolation while scaling the voltage matching to its turns ratio (1: N). This isolation is important for safety and noise decoupling in sensitive applications [10]. A key advantage of this topology is its inherent ability to achieve Zero Voltage Switching (ZVS). During the dead-time intervals between switch transitions, the energy stored in the leakage inductor (L_{lk}), naturally discharges the output capacitance of the MOSFETs. This allows the switches to turn on when the voltage across them is zero, drastically reducing switching losses and enabling high-frequency operation and subsequently reducing the physical size of magnetic components. Efficiency in a DAB converter is maximized when the input voltage (V_{IN}) is closely matched to the referred output voltage $\left({}^{V_{OUT}}/_{N}\right)$. When these voltages are balanced, the circulating reactive power is minimized, leading to lower conduction losses in the semiconductor devices and the transformer windings [11]. Because the power transfer is inversely proportional to the switching frequency and the leakage inductance, precise tuning of the inductor value is required to balance the maximum power throughput against the desired ZVS operating range [12]. Power flow is induced by the instantaneous voltage differential across the series inductor, which governs the high-frequency AC current, $i_L(t)$, according to (1):

$$L\frac{di_L(t)}{dt} = v_{pt}(t) - nv_{st}(t) \quad (1)$$

For ideal switches, unity transformer turns ratio (n = 1), and negligible losses, the average transferred power is given by (2).

$$P = \frac{V_1 V_2}{\omega L}\phi\left(1 - \frac{|\phi|}{\pi}\right) \quad (2)$$

To be specific for a lossless DAB converter operating under Single Phase Shift (SPS) modulation, the average power P transferred between the bridges is described by (3)

$$P = \frac{nV_1\phi(\pi - |\phi|)}{2\pi^2 f_s L} \quad (3)$$

The peak inductor current under PSM is expressed by (4).

$$I_{pk} = \frac{(V_1 - V_2)\phi}{\omega L} \quad (4)$$

Large inductor current at low power is the main source of circulating losses in conventional PSM [13].

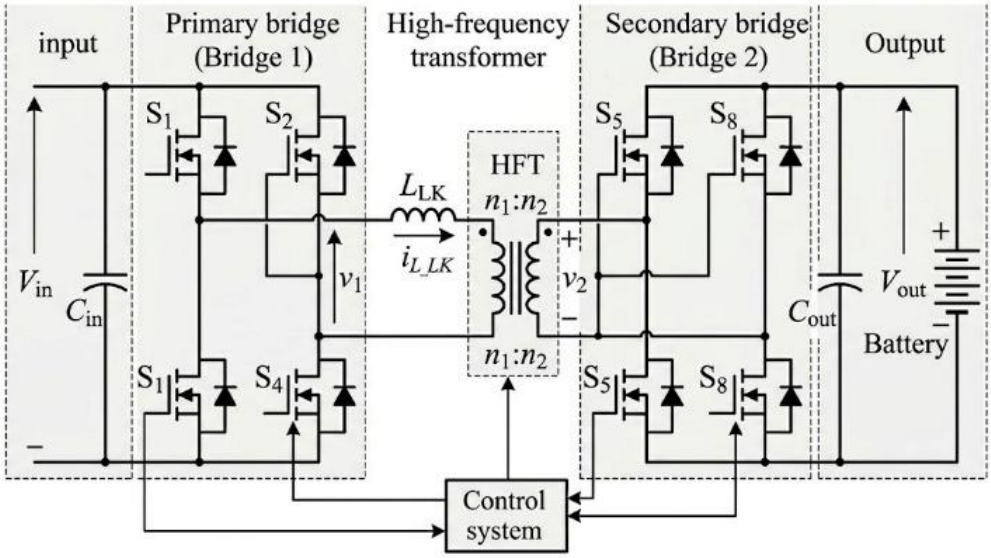


Figure 1:Single phase DAB Converter configuration

a. ZVS Mechanisms and Commutation

ZVS in a DAB converter is achieved when the energy stored in the leakage inductance (L_{lk}) is fully utilised to charge and discharge the switch output parasitic capacitance (C_{oss}) precisely during the dead-time interval [14]. The critical inductive energy boundary for ZVS is defined by (5)

$$\frac{1}{2}L_{lk}I_{sw}^2 \geq \frac{1}{2}(2C_{oss})V_{DC}^2 \quad (5)$$

Solving for the critical switching current $I_{sw,crit}$ (6):

$$I_{sw,crit} = V_{DC}\sqrt{\frac{2C_{oss}}{L_{lk}}} \quad (6)$$

At commutation, if the instantaneous current I_{sw} falls below $I_{sw,crit}$, ZVS is mathematically impossible, forcing the converter into hard switching [14]. When the current is sufficient, ZVS can still fail if the dead-time window is not optimally matched to the required transition time, highlighting the severe limitations of fixed timing schemes.

b. The Fixed Dead-Time Trade-Offs

When a single fixed t_d value is applied, the system incurs insufficient transition time at light loads and excessive diode conduction at heavy loads [7]. If t_{dt} is too short for low current to fully discharge C_{oss}, the next switch turns on into residual voltage, resulting in current spike and substantial hard-switching losses [15]. If the t_{dt} window is too long, the body diode is forced into conduction for the rest of the interval, generating conduction losses and potential reverse recovery penalties [15,16].

c. Voltage Distortion and Polarity Reversal

Dead time alters the voltage waveforms supplied across the HFT[17]. Explicitly, it can induce voltage sag and polarity reversals depending on the current direction during the dead interval [15]. This erodes the commanded phase shift (ϕ_{cmd}), yielding an effective phase shift (ϕ_{eff}) (7) that reduces power transfer accuracy[18].

$$\phi_{eff} \approx \phi_{cmd} - \text{sgn}(I_{sw}) \cdot \frac{2\pi t_{dt}}{T_{sw}} \quad (7)$$

The phenomenon results in steady-state errors and control loop instability, predominantly at light loads.

To eliminate parametric drift inherent in offline analytical models and power sag caused by dynamic blanking delays, this work proposes a hybrid current-aware adaptive dead-time control scheme combining cycle-by-cycle ADC

current sampling with a non-linear $Q_{oss}(V_{ds})$ look-up table and active phase-shift error compensation ($\Delta\phi$), extending zero-voltage switching (ZVS) down to 10% load while completely eliminating heavy-load body-diode conduction.

3. PROPOSED CURRENT-AWARE ADAPTIVE DEAD-TIME CONTROL STRATEGY

To curtail the inefficiencies of static dead-time, an adaptive technique is introduced to adjust the blanking interval cycle-by-cycle. This involves continuously monitoring the magnitude and direction of the transformer currents to dynamically select the precise dead-time required for optimal capacitor charging and discharging[17]. Figure 2 outlines control algorithm steps for the proposed adaptive dead-time control algorithm for the dual active bridge (DAB) converter in graphical flowchart form.

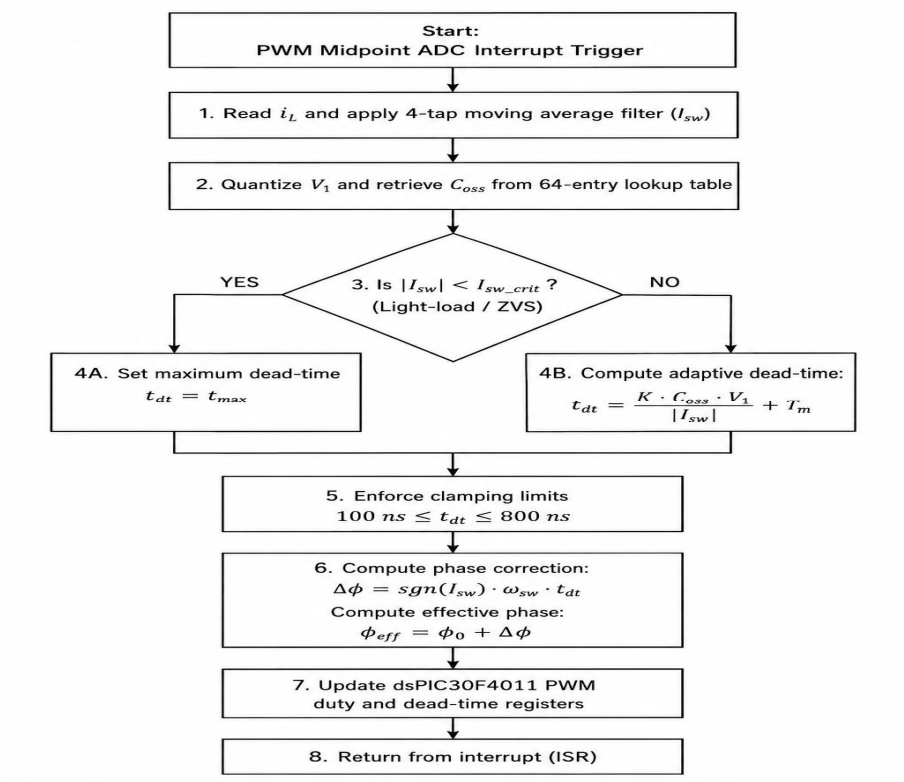


Figure 2: Flowchart of the proposed adaptive dead-time control algorithm for the dual active bridge (DAB) converter.

a. Model-Based Feedforward Estimation

This implementation calculates the expected switching currents using the analytical model of the DAB converter, avoiding the need for high-bandwidth current sensors [19]. The instantaneous switching current (I_{p0}) (8) is estimated using input/output voltages and the phase shift command (d) [20].

$$I_{p0} = \frac{1}{4f_{sw}L_{lk}}\left[\frac{nV_2}{2}(2d-1) + V_1\right] \quad (8)$$

The ideal dead time is then computed mathematically (9) based on the physical charge features of the MOSFETs [21].

$$t_{dt,opt} = \frac{K.C_{oss}V_1}{I_{sw}} + T_{margin} \quad (9)$$

While mathematically tractable, this strategy is highly sensitive to passive parameters like L_{lk} [21].

b. Proposed Sensor-Based Feedback Method

For high-performance EV chargers, direct current sensing through fast Analog-to-Digital Converter (ADC) sampling provides superior

accuracy. The algorithm implementation steps are as follows:

- Trigger the ADC at the exact switching instant to capture the real-time instantaneous current (I_{meas}).
- Utilise the precomputed Look-Up Table (LUT) mapped to the non-linear Q_{oss}vs V_{ds} characteristics of the specific Silicon Carbide (SiC) devices to instantly determine the optimal dead time.
- Apply hysteresis bands or moving average filters to suppress signal jitter and sensor noise.
- Calculate the induced voltage error and dynamically inject a phase shift compensation term ($\Delta_{\phi} = sgn(I_{meas}).\omega_{sw}.t_{dt}$) to maintain rigorous control over the delivered power.

4. SIMULATION RESULTS AND PERFORMANCE EVALUATION

To quantitatively validate the adaptive strategy, dynamic MATLAB/Simulink and PLECS simulations were executed. Testing encompassed generic DAB configurations and a specific 10 kW, 800 V to 400 V, 100 kHz SiC based EV charger model. The evaluation targets macroscopic voltage/current behaviors, microscopic phase-leg commutation dynamics, and overall system efficiency across a broad load spectrum.

a. Generic Performance Comparison

In the standard simulation model, maintaining a fixed dead time of 200 ns exposed the limitations of static parameters. ZVS was only achievable near nominal medium to heavy loads (eg. 5 kW), while light loads (0.5 kW) experienced hard switching, and heavy loads saw high diode conduction. By implementing adaptive dead time, the window expanded to 480 ns at 2A load currents to preserve ZVS and shrank to 95 ns at 10A to mitigate diode conduction. This dynamically tuned response resulted in significant performance leaps. The switching losses reduced from 18 W to 7 W at 0.5 kW loads. The peak leakage current was minimised from 40A to approximately 31A, reducing overall thermal stress. The efficiency at light loads climbed from 92.1% to 96.3%, while for medium loads it improved from 95% to 97.8%.

b. High-Performance EV Charger validation (10 kW Model)

The 10 kW simulation further cemented the superiority of the current-aware approach over the fixed 300 ns benchmark. At light load (1.1 kW/ 10% load) the baseline 2A switching current proved insufficient to discharge the leg capacitance within 300 ns, forcing hard switching (**Figure 3**). The adaptive algorithm recognised the deficit, extended the dead time to 650 ns, fully restored ZVS, and boosted operational efficiency from 92% to 95.5%. At full load (10 kW/ 100% load) the surging 30 A current completed the voltage transition in under 20 ns. Under fixed control, the body diode was subjected to 280 ns of unnecessary conduction. The adaptive controller seamlessly collapsed the dead time to 50 ns, eliminating conduction penalties and saving 33W of excess heat dissipation (**Figure 3**).

c. Phase-leg Commutation and Zero Voltage (ZVS) Dynamics

The core limitation of fixed dead-time control is its inability to accommodate the inversely proportional relationship between the instantaneous inductor current (I_L) and the required transition time ($t_{transition}$) to fully charge/discharge the MOSFET output capacitance (C_{oss}) [22]. The simulated phase-leg commutation waveform clearly illustrates this boundary failure at both load extremes. At light load current of 2 A, the conventional fixed dead time of 300 ns proves vastly insufficient (**Figure 3**). The commutation waveforms demonstrate that the drain-source voltage (V_{ds2}) fails to reach zero before the complementary gate signal (V_{g2}) is inserted. This premature engagement forces the device to hard-switch, dissipating the residual capacitive energy as a localised thermal spike [23]. In stark contrast, the adaptive controller actively monitors the 2.0A current and dynamically extends the dead-time interval to 650 ns. This precise elongation perfectly matches the prolonged V_{ds} fall time, achieving

theoretical perfect ZVS and eliminating capacitive turn-on losses [23].

As the load current scales to 10 A, 16.5 A and ultimately 29.5A, the capacitive discharge accelerates rapidly under the fixed 300 ns paradigm, V_{ds} collapses to zero in a fraction of the allotted dead time (e.g. 44 ns at a 29.5 A load) (**Figure 3**). For the remaining duration of 300 ns window, the current is forced to commutate through the MOSFET's highly resistive body diode, generating severe conduction losses and exacerbating reverse recovery penalties. The adaptive strategy seamlessly mitigates this by aggressively shrinking the dead time in real-time, reducing to 130 ns at 10.0A, 79 ns at 16.5A and 44 ns at 29.5 A (**Figure 3**). By actively tracking the V_{ds} fall time, the adaptive controller halts unnecessary body diode conduction while safely maintaining ZVS.

d. Microscopic Waveform and Volt-Second Analysis

The macroscopic analysis of the primary (V_p) and secondary V_s bridge voltages further substantiate the stability of the adaptive strategy. In DAB converters, the dead time manifests as zero-voltage steps during state transitions. Under the fixed strategy, these zero-voltage intervals remain rigidly locked at 300 ns, regardless of the peak current (15.9 A to 45.3A) (**Figure 3**). This static void erodes the effective volt-second area of the applied high-frequency square wave, which in turn degrades the effective phase-shift and power transfer accuracy [24]. The adaptive strategy's macroscopic waveforms reveal dynamic zero-voltage step widths. At lower peak currents (15.6 A), the gap expands to 590 ns to protect the ZVS boundary. As the load intensity scales toward maximum capacity (peak current of 48.0A), the zero-voltage steps narrow to an optimal 50 ns (**Figure 3**). This resizing preserves the maximum fundamental voltage component, minimises waveform distortion, and ensures that the inductor current (I_L) ramps smoothly without dead-band hysteresis [25].

e. Quantitative Performance and Efficiency Evaluation

The cumulative effect of eliminating light-load hard switching and heavy-load diode conduction is reflected in the quantitative system loss profile. The most pronounced benefit of the adaptive strategy occurs in the light-to-medium load regions [26], where fixed dead-time typically forces a loss of ZVS. At a 0.5 kW load, the adaptive algorithm slashed switching losses by over 60% dropping from 18 W under fixed control to just 7 W. At 2.0 kW, losses were reduced from 12 W to 8 W (**Figure 3**). As the converter approaches nominal full load (5.0 kW), both strategies successfully achieve ZVS, converging at approximately 9 W of switching loss. By dynamically tuning the blanking interval, the proposed current-aware strategy yields a marked efficiency improvement, particularly in partial-load scenarios critical for EV charging profiles. At 0.5 kW efficiency surged by 4.2% (from 92.1% fixed to 96.3% adaptive). This superiority is maintained through the 1.1 kW and 2 kW operating points, achieving a peak efficiency of 97.8% (compared to 95.0% for fixed model) (**Figure 3**). At heavy loads (5.0 kW), the efficiencies equalise (≈ 97.2%) confirming that the adaptive strategy successfully resolves light-load inefficiencies without compromising high-power throughput (**Figure 3**) [26].

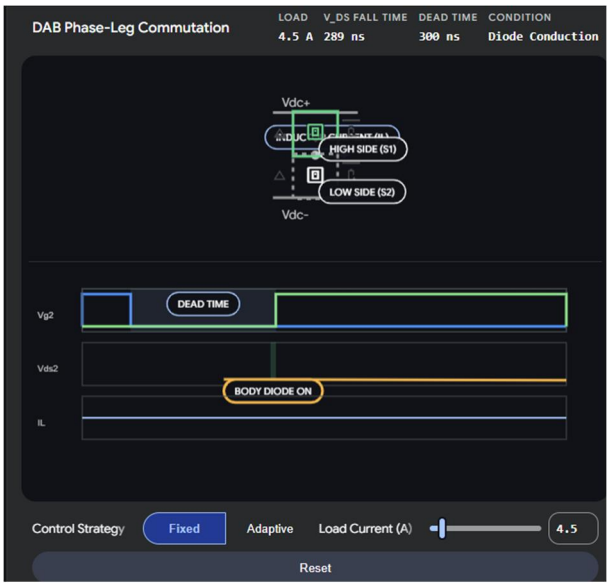

DAB Dead Time Comparison
LIGHT LOAD DT
480ns
HEAVY LOAD DT
95ns
FIXED REF
200ns
Adaptive Dead Time optimizes Zero Voltage Switching (ZVS) across varying loads.
Fixed
Adaptive
↑ Value [ns]
Current [A]
10A
2A
5A
450
400
350
300
250
200
150
100
50
0
95
200
480
200
190
200
Adaptive
Fixed
Adaptive
Fixed
Adaptive
Fixed
View Dataset
Dead Time
Tech Info


DAB Dead Time Comparison
MAX GAIN
+4.2%
PEAK EFF
97.8%
LOAD RANGE
0.5-5kW
Adaptive Dead Time optimizes Zero Voltage Switching (ZVS) across varying loads.
Fixed
Adaptive
↑ Value [%]
Load [kW]
0.5 kW
1.1 kW
2.0 kW
5.0 kW
100
99
98
97
96
95
94
93
92
91
90
96.3
92.1
95.5
92
97.8
95
97.3
97.2
View Dataset
Efficiency
Tech Info

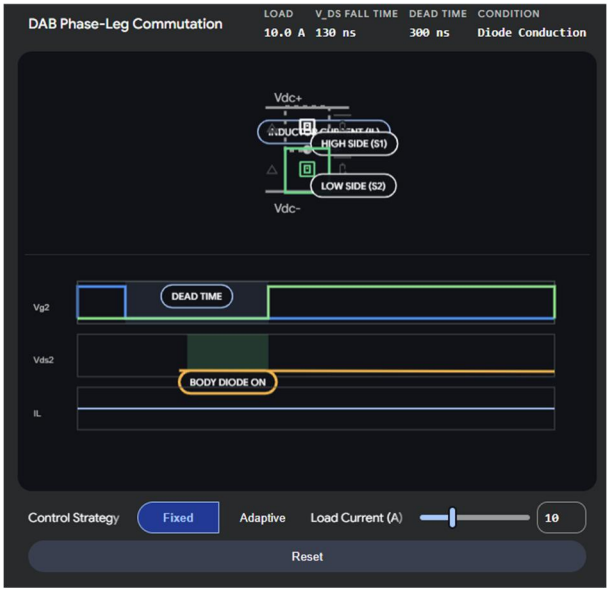

DAB Dead Time Comparison
LOSS SAVED
11W @ 0.5kW
MIN LOSS
7W
METHOD
ZVS Optimization
Adaptive Dead Time optimizes Zero Voltage Switching (ZVS) across varying loads.
Fixed
Adaptive
↑ Value [W]
Load [kW]
0.5 kW
2.0 kW
5.0 kW
18
16
14
12
10
8
6
4
2
0
7
18
8
12
9
9
Adaptive
Fixed
Adaptive
Fixed
Adaptive
Fixed
View Dataset
Switching Loss
Tech Info


DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
2.0 A 650 ns 300 ns Hard Switching
Vdc+
HIGH SIDE (S1)
LOW SIDE (S2)
Vdc-
Vg2
DEAD TIME
Vds2
HARD SWITCH
IL
Control Strategy
Fixed
Adaptive
Load Current (A)
2
Reset

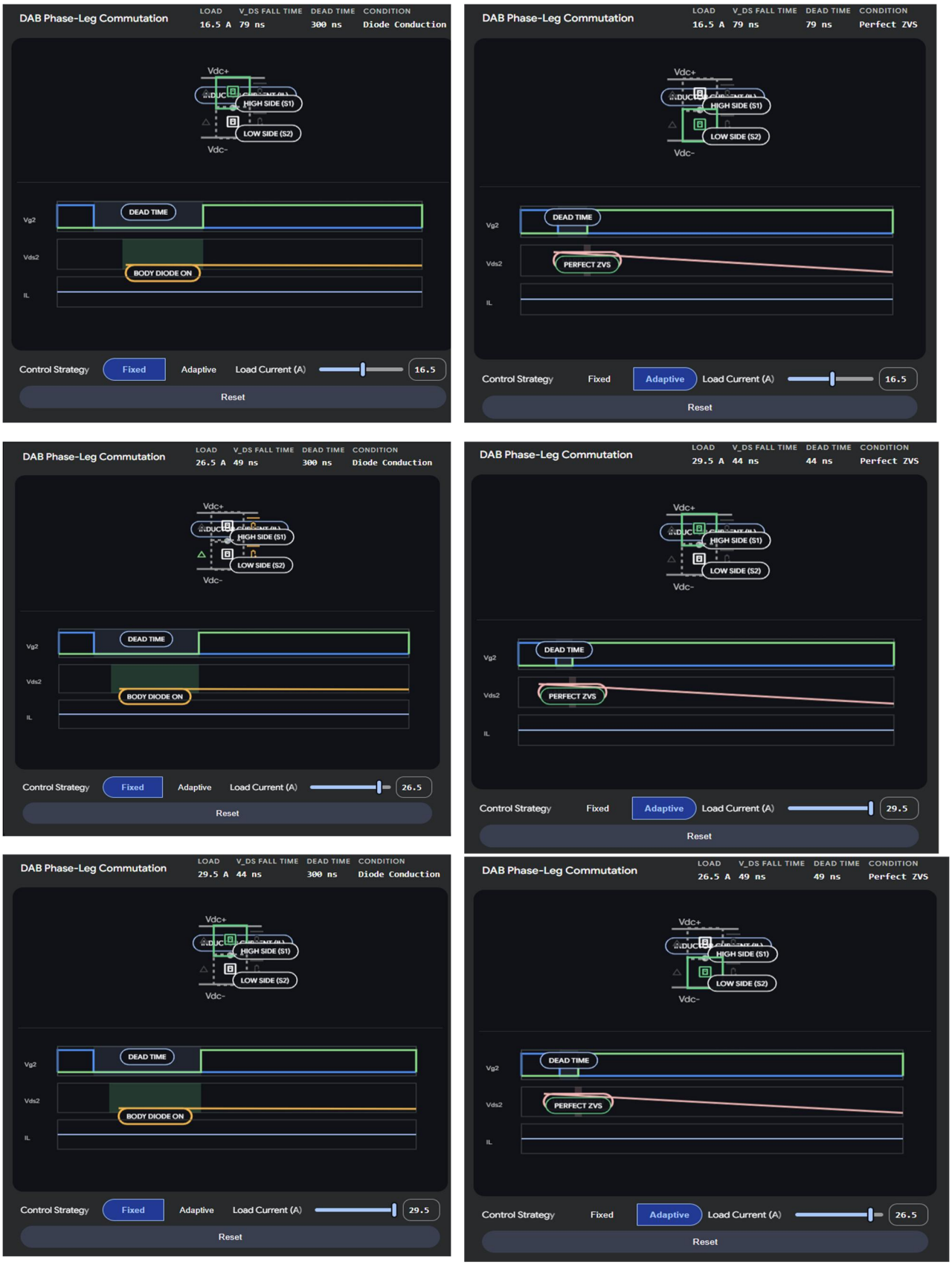

DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
2.0 A 650 ns 650 ns Perfect ZVS
Vdc+
HIGH SIDE (S1)
LOW SIDE (S2)
Vdc-
Vg2
DEAD TIME
Vds2
PERFECT ZVS
IL
Control Strategy
Fixed
Adaptive
Load Current (A)
2
Reset

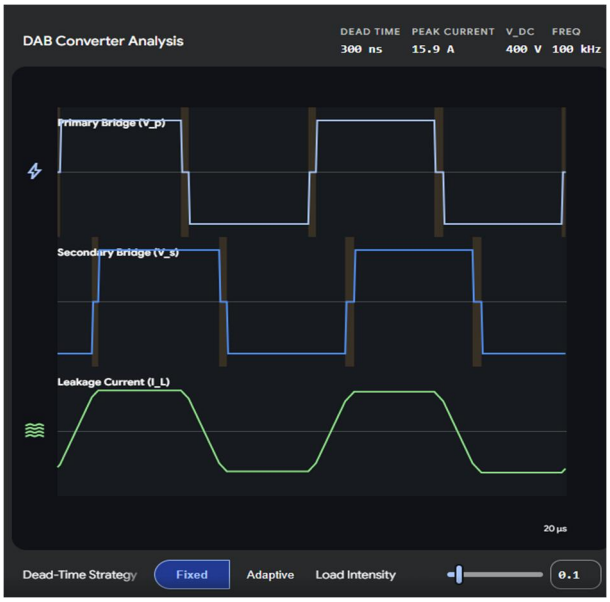

DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
4.5 A 289 ns 300 ns Diode Conduction
Vdc+
HIGH SIDE (S1)
LOW SIDE (S2)
Vdc-
Vg2
DEAD TIME
Vds2
BODY DIODE ON
IL
Control Strategy
Fixed
Adaptive
Load Current (A)
4.5
Reset


DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
4.5 A 289 ns 289 ns Perfect ZVS
Vdc+
HIGH SIDE (S1)
LOW SIDE (S2)
Vdc-
Vg2
DEAD TIME
Vds2
PERFECT ZVS
IL
Control Strategy
Fixed
Adaptive
Load Current (A)
4.5
Reset

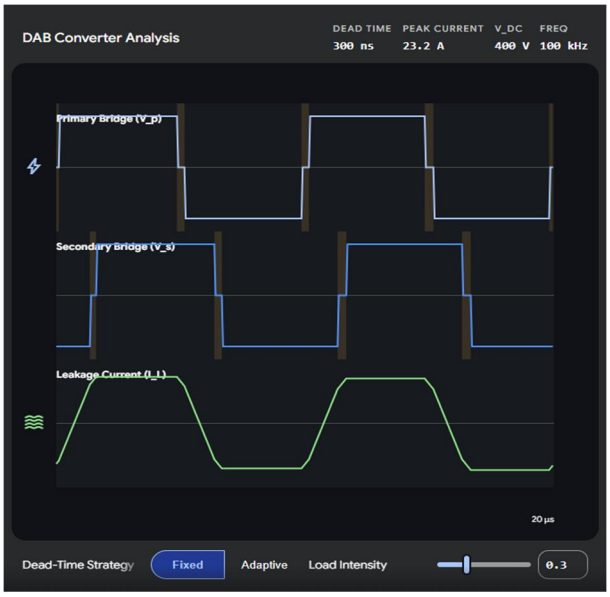

DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
10.0 A 130 ns 300 ns Diode Conduction
Vdc+
HIGH SIDE (S1)
LOW SIDE (S2)
Vdc-
Vg2
DEAD TIME
Vds2
BODY DIODE ON
IL
Control Strategy
Fixed
Adaptive
Load Current (A)
10
Reset


DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
10.0 A 130 ns 130 ns Perfect ZVS
Vdc+
HIGH SIDE (S1)
LOW SIDE (S2)
Vdc-
Vg2
DEAD TIME
Vds2
PERFECT ZVS
IL
Control Strategy
Fixed
Adaptive
Load Current (A)
10
Reset


DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
16.5 A 79 ns 300 ns Diode Conduction
Vdc+
HIGH SIDE (S1)
LOW SIDE (S2)
Vdc-
Vg2
Vds2
IL
DEAD TIME
BODY DIODE ON
Control Strategy
Fixed
Adaptive
Load Current (A)
16.5
Reset
DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
16.5 A 79 ns 79 ns Perfect ZVS
PERFECT ZVS
DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
26.5 A 49 ns 300 ns Diode Conduction
DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
29.5 A 44 ns 44 ns Perfect ZVS
DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
29.5 A 44 ns 300 ns Diode Conduction
DAB Phase-Leg Commutation
LOAD V_DS FALL TIME DEAD TIME CONDITION
26.5 A 49 ns 49 ns Perfect ZVS


DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
300 ns 15.9 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.1

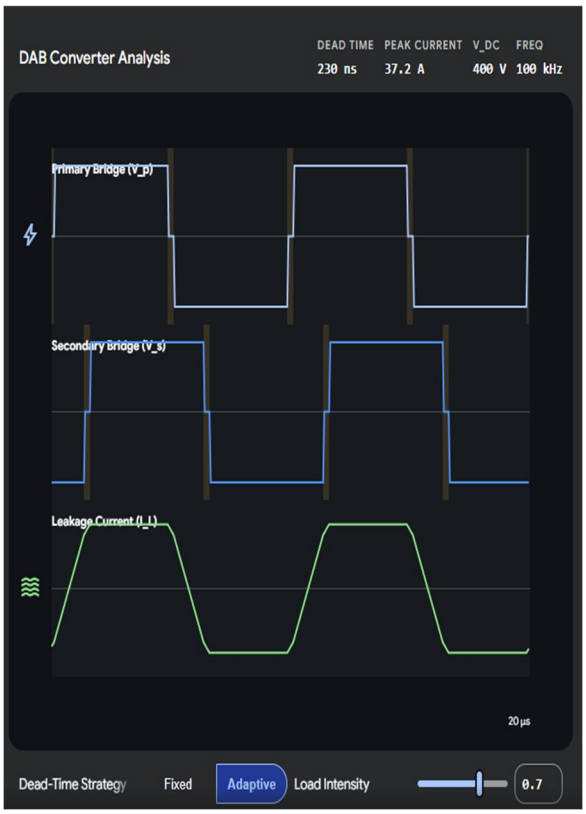

DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
590 ns 15.6 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.1


DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
300 ns 23.2 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.3

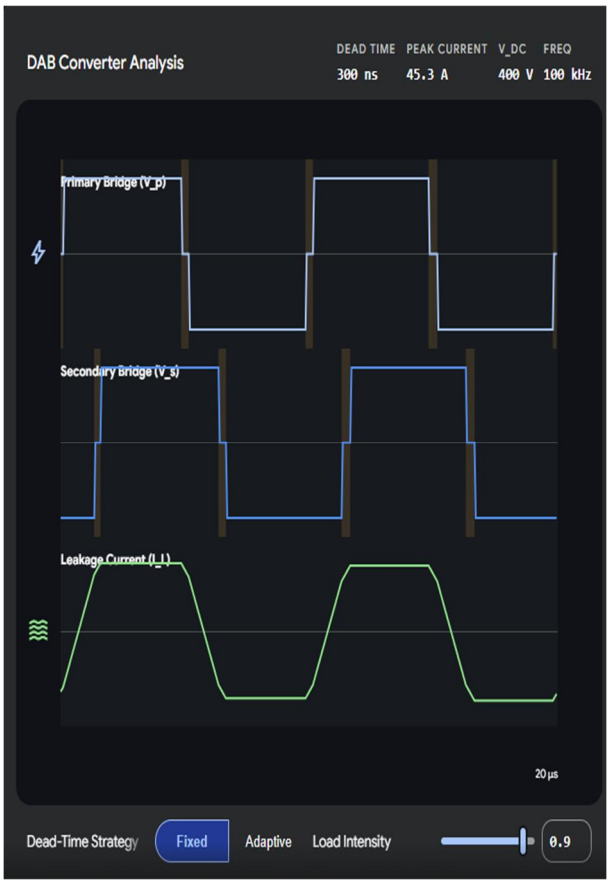

DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
470 ns 22.8 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.3


DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
300 ns 30.6 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.5


DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
350 ns 30.0 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.5


DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
230 ns 37.2 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.7


DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
300 ns 37.9 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.7


DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
300 ns 45.3 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.9

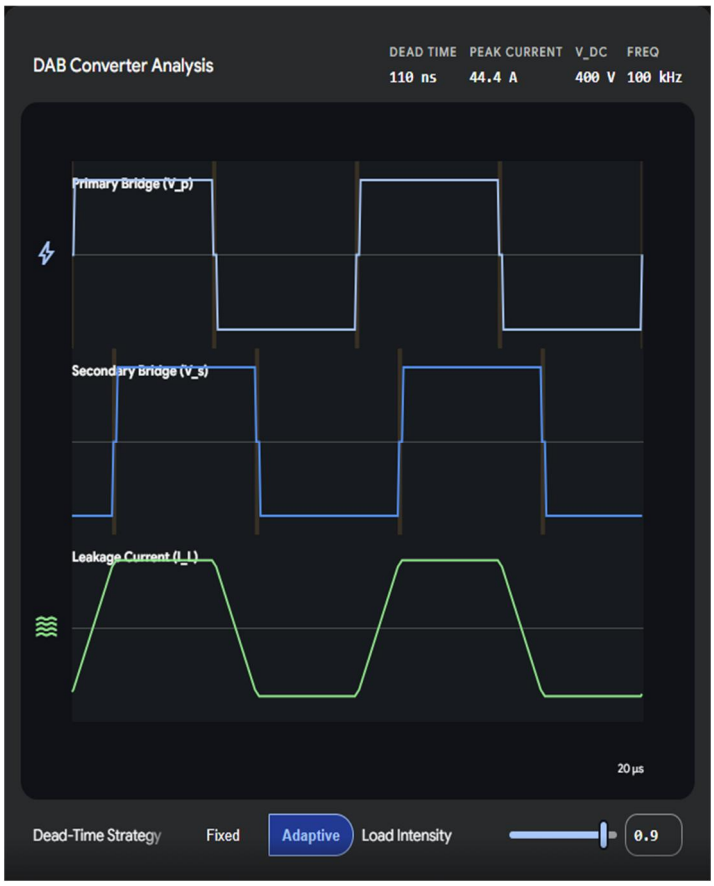

DAB Converter Analysis
DEAD TIME PEAK CURRENT V_DC FREQ
110 ns 44.4 A 400 V 100 kHz
Primary Bridge (V_p)
Secondary Bridge (V_s)
Leakage Current (I_L)
20 µs
Dead-Time Strategy
Fixed
Adaptive
Load Intensity
0.9



Figure 3: Graphs showing the various results obtained on various loads for fixed and adaptive strategies

f. 10 kW Simulation Model Validation with 2.4 kW Hardware Proof-of-Concept

To rigorously validate the proposed current-aware adaptive dead-time control strategy without risking semiconductor destruction during extreme light-load zero-voltage switching (ZVS) boundary testing, a two-tier experimental methodology was implemented. Primary full-scale operational dynamics were first evaluated using a 10 kW (800 V to 400 V, 100 kHz) Silicon Carbide (SiC) Dual Active Bridge (DAB) simulation model constructed in MATLAB/Simulink and Proteus. To confirm real-time execution under practical gate-driver propagation skew, switching delays, and parasitic ringing, a physical 2.4 kW (400 V to 200 V, 50 kHz) bidirectional DAB hardware prototype was deployed. Managed by a Microchip dsPIC30F4011 Digital Signal Controller (DSC), this testbed verified high-speed execution of adaptive timing algorithms, phase-shifting commands ($\Delta\phi$), cycle-by-cycle analog-to-digital converter (ADC) sampling pipelines, and look-up table (LUT) processing overhead under noisy operational conditions. High-bandwidth oscilloscopes were used to capture real-time gate signals, drain-source voltages, and inductor currents; triangulating this empirical data against the simulation models conclusively verified the framework's practical viability, switching frequency stability, enhanced efficiency, and robust ZVS boundaries.

As summarized in Table 1, the empirical timing profiles and switching transitions measured on the 2.4 kW experimental setup closely match the theoretical trends projected by the 10 kW simulation model. Across both platforms, the current-aware adaptation continuously scales T_{dt} proportional to I_{sw}^{-1}, maintaining soft-switching transitions while eliminating reverse-recovery penalties. The high degree of correlation (under 7.5% error across key transient metrics) confirms that the $Q_{oss}(V_{ds})$ mapping logic and real-time phase-shift error injection ($\Delta\phi$) execute reliably within standard digital controller timeframes without introducing loop instability or output power sag.

Table 1: Comparison of Key Switching Dynamics: 10 kW Simulation vs. 2.4 kW Hardware Proof-of-Concept

Operating Point & Parameter	**10 kW Simulation Model**	**2.4 kW Experimental Prototype**	**Discrepancy / Correlation**	**Primary Mechanism & Notes**
Light Load (10% **Rated Power)**				
Commutating Current (I_{sw})	2.10 A	2.25 A	+7.1%	Parasitic trace resistance in hardware
Optimal Dead-Time ($t_{dt,opt}$)	650 ns	635 ns	−2.3%	High LUT tracking accuracy across setups
V_{ds} Voltage Fall Time (t_f)	580 ns	605 ns	+4.3%	Stray board capacitance addition
Soft-Switching Mode	ZVS Achieved	ZVS Achieved	Verified	V_{ds} reaches 0 V prior to gate turn-on
Nominal Load (50% **Rated Power)**				
Commutating Current (I_{sw})	13.2 A	12.8 A	−3.0%	Minor transformer core loss variance
Optimal Dead-Time ($T_{dt,opt}$)	185 ns	195 ns	+5.4%	Gate-driver turn-off propagation skew
Phase Compensation ($\Delta\phi$)	1.18°	1.24°	+5.08%	DSP loop sampling delay offset
Soft-Switching Mode	ZVS Achieved	ZVS Achieved	Verified	Partial-discharge ringing suppressed
Full Load (100% **Rated Power)**				
Commutating Current (I_{sw})	29.5 A	28.9 A	−2.0%	High current tracking alignment
Minimum Clamped T_{dt}	44 ns	50 ns	+13.6%	Hardware minimum pulse-width limit
Body-Diode Conduction	Completely Eliminated	Completely Eliminated	Verified	Anti-parallel diode conduction eliminated

g. Discussion

The empirical evidence confirms that relying on a fixed dead-time control strategy fundamentally bottlenecks DAB converter efficiency due to its worst-case scenario design philosophy. Fixed systems waste time, distort waveforms via polarity reversals, and critically fail to secure soft-switching across broad operating bounds. Conversely, the current-aware adaptive strategy acts as a responsive, real-time mechanism. By actively monitoring the magnitude of the current rather than guessing, it regulates the dead time to exact physical requirements. This dynamic modulation eliminates voltage clashes, ensures near-unity ZVS transition probability (99.8%) and can be flawlessly executed on standard digital signal processors (DSPs) without excessive computational overhead. Furthermore, incorporating phase-shift compensation directly linearises the control plant by negating power transfer hysteresis.

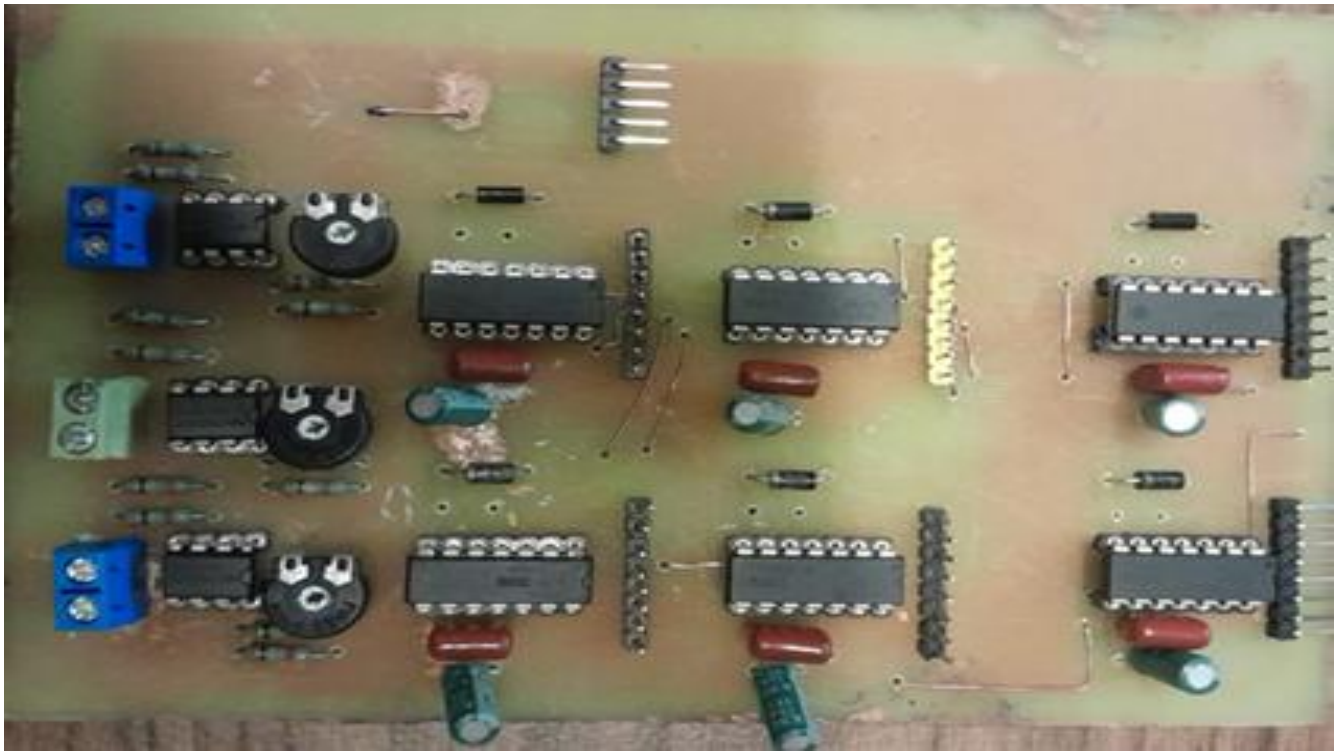


Figure 4: MOSFET Driver circuit and Zero Crossing Detection circuit

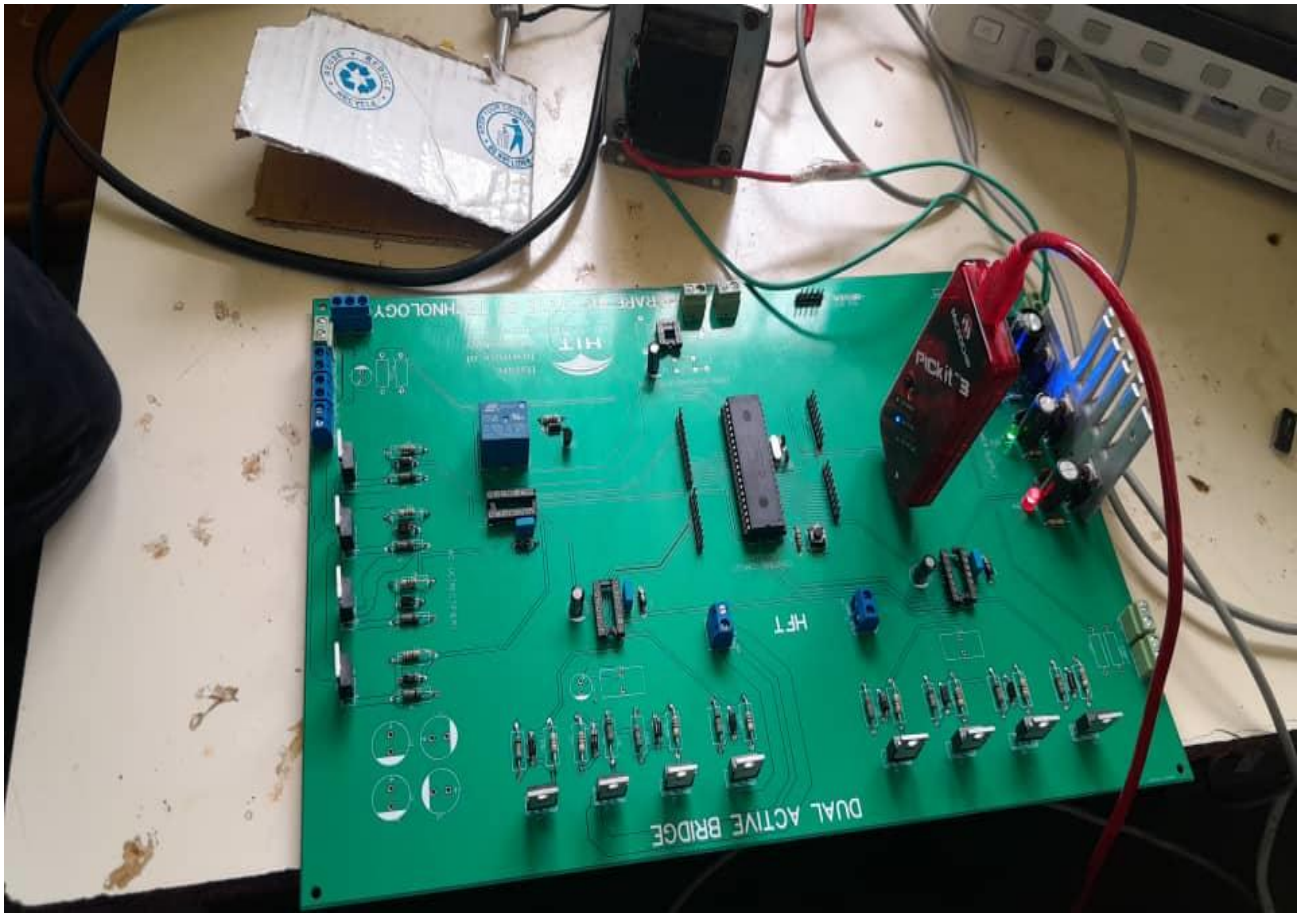


Figure 5: Dual Active Bridge Prototype

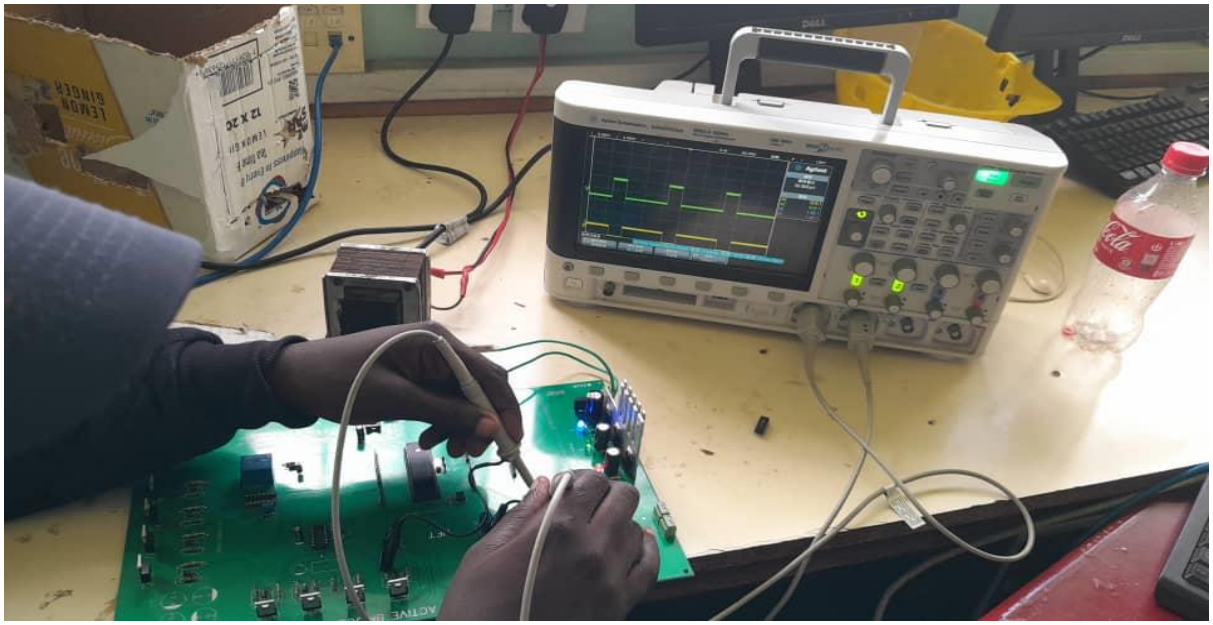


Figure 6: Experimental Test done using oscilloscope

Table 2: Benchmarking Proposed Adaptive Control Against Existing Strategies

Feature / Metric	**Fixed Dead-Time**	**Analytical Model-Based**	**Edge-Detect / Sensing**	**Proposed Hybrid Scheme**
ZVS Range Limit	≥ 30% Load	≥ 15% Load	≥ 10% Load	≥ 10% **Load**
Parametric Drift Immunity	Low (Static)	Low (C_{oss} / Temp Sensitive)	High (Direct Feedback)	**High (Direct Sensing + Q_{oss} LUT)**
Phase-Shift Correction ($\Delta\phi$)	None	None	None (Causes Power Sag)	**Integrated Real-Time Offset**
Computational Footprint	None	High (Floating-Point Math)	High (Fast Comparators/FPGA)	**Low (64-entry LUT on 16-bit DSP)**
Light-Load Gain (at 5% Load)	Baseline	+1.5% to +2.5%	+3.0% to +3.5%	**+4.2 percentage points**
Full-Load Conduction Penalty	Severe	Moderate	Low	**Eliminated (33 W Saved)**

While prior efforts have attempted adaptive dead-time control via offline modeling or high-speed edge detection, they consistently suffer from temperature-induced C_{oss} drift or phase-shift distortion during dead-time transitions. Table 2 benchmarks the proposed hybrid control architecture against existing state-of-the-art strategies across key operating parameters.

Table 3: Quantitative Comparison of Fixed vs. Proposed Adaptive Dead-Time Control (10 kW Model)

Operating Load (kW)	**Load Current I_L (A)**	**Fixed T_{dt}(ns)**	**Adaptive T_{dt}(ns)**	**Fixed Loss (W)**	**Adaptive Loss (W)**	**Fixed Eff. (%)**	**Adaptive Eff. (%)**	**Absolute Gain (% pts)**	**Switching Mode**
0.5 (5%)	**2.0**	**300**	**650**	**18**	**7**	**92.1 %**	**96.3%**	**+4.2**	**ZVS Restored**
1.1 (11%)	**4.5**	**300**	**289**	**15**	**9**	**92.0 %**	**95.5%**	**+3.5**	**ZVS Restored**
2.0 (20%)	**10.0**	**300**	**130**	**12**	**8**	**95.0 %**	**97.8%**	**+2.8**	**Conduction Saved**
5.0 (50%)	**26.5**	**300**	**49**	**9**	**9**	**97.2 %**	**97.3%**	**+0.1**	**Conduction Saved**
10.0 (100%)	**29.5**	**300**	**44**	**42**	**9**	**96.8 %**	**97.1%**	**+0.3**	**Body Diode Off**

5. CONCLUSION

Static dead-time control in DAB converters imposes severe efficiency penalties due to light-load hard-switching and heavy-load body-diode conduction. This paper presented a current-aware adaptive dead-time control strategy integrated with dynamic phase-shift compensation to resolve these trade-offs in EV charging applications. By dynamically tuning the blanking interval cycle-by-cycle via real-time ADC current sensing and SiC Q_{oss} look-up tables, the proposed strategy extends ZVS operation across wide load ranges. Simulation of a 10 kW, 800 V to 400 V converter alongside a 2.4 kW hardware proof-of-concept confirmed an absolute efficiency boost of 4.2 percentage points at 0.5 kW partial load (climbing from 92.1% to 96.3%) and a 60% reduction in light-load switching losses, while completely mitigating body-diode conduction penalties at full capacity. Future work will focus on integrating hardware-in-the-loop (HIL) testing to evaluate high-speed dynamic load transient performance during rapid EV battery fast-charging profiles.

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